CubeSat Kit™

Pluggable Socketed Processor Module (PSPM) E

Hardware Revision: B

PSPM for Microchip® PIC24 w/USB OTG and CubeSat Kit Development Board

Applications

- nanoLab Kit™
- CubeSat nanosatellite control, C&DH, TT&C
- General-purpose low-power computing for CubeSat Kit architecture
- Remote sensing for harsh environments

Features

- For CubeSat Kit Development Board (DB)
- For Microchip® PIC24FJ256GB210 16-bit microcontroller (MCU)[1]
- 8.000MHz & 32.768kHz clock crystals
- AT25DF641 64Mbit SPI serial Flash memory
- Independent latchup (device overcurrent) protection
- Independent external reset supervisor (POR/BOR)
- With 100-pin clamshell ZIF socket
- 4-layer gold-plated green-soldermask PCB
- Compatible with Pumpkin's Salvo™ RTOS and HCC-Embedded's EFFS-THIN SD Card file FAT file system for ease of programming

ORDERING INFORMATION

Pumpkin P/N 710-00711

Option Code	PPM Connector Height
/00 (standard)	+6mm

Contact factory for availability of optional configurations.
Option code /00 shown.

CAUTION

Electrostatic Sensitive Devices

Handle with Care

[1] For a list of integrated peripherals and other controller-specific features when PSPM E is outfitted with a particular processor, see the CubeSat Kit PPM E1 datasheet.

CHANGELOG

Rev.	Date	Author	Comments
A	20110731	AEK	Initial revision.

OPERATIONAL DESCRIPTION

PSPM E enables CubeSat Kit and nanoLab Kit customers to utilize a PIC24 with integrated USB on a CubeSat Kit Development Board (DB). With its 100-pin clamshell ZIF socket, PSPM E accepts the 100-pin PIC24FJ256GB210-I/PF, with a wide selection of on-chip peripherals. Additionally, a 64Mbit external serial Flash memory is present for off-chip storage.

PSPM E is fitted with a micro-AB USB connector and a jumper-based selector that enables the use of the micro-AB USB connector or the type B USB connector on a paired DB or Motherboard (MB) for USB connectivity.

When fitted with a PIC24FJ256GB210-I/PF, PSPM E is electrically identical to PPM E1.

Note: PSPM E is not compatible with the PIC24FJ256GA110 – use PSPM D instead. It is not intended for use with dsPIC33 devices – use PSPM D instead. Lastly, it is not compatible with the PIC24FJ256GB110 due to a difference in physical chip sizes.[2]

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Operating temperature	T_A	-40 to +85	ºC
Voltage on **+5V_USB** bus		-0.3 to +6.0	V
Voltage on **+5V_SYS** bus			
Voltage on **–FAULT_OC** open-collector output			
Voltage on **VCC** bus		-0.3 to +3.6	V
Voltage on **VCC_SD** bus			
Voltage on any mixed analog/digital processor I/O pin		-0.3 to (**VCC** + 0.3)	V
Voltage on any digital-only processor I/O pin		-0.3 to 6.0	
DC current through any pin of PPM connector **H1**	I_{PIN_MAX}	1.2	A

Refer to the Microchip® PIC24FJ256GB210 family datasheet for additional absolute maximum ratings associated with processor **U1**, especially per-pin current limits.

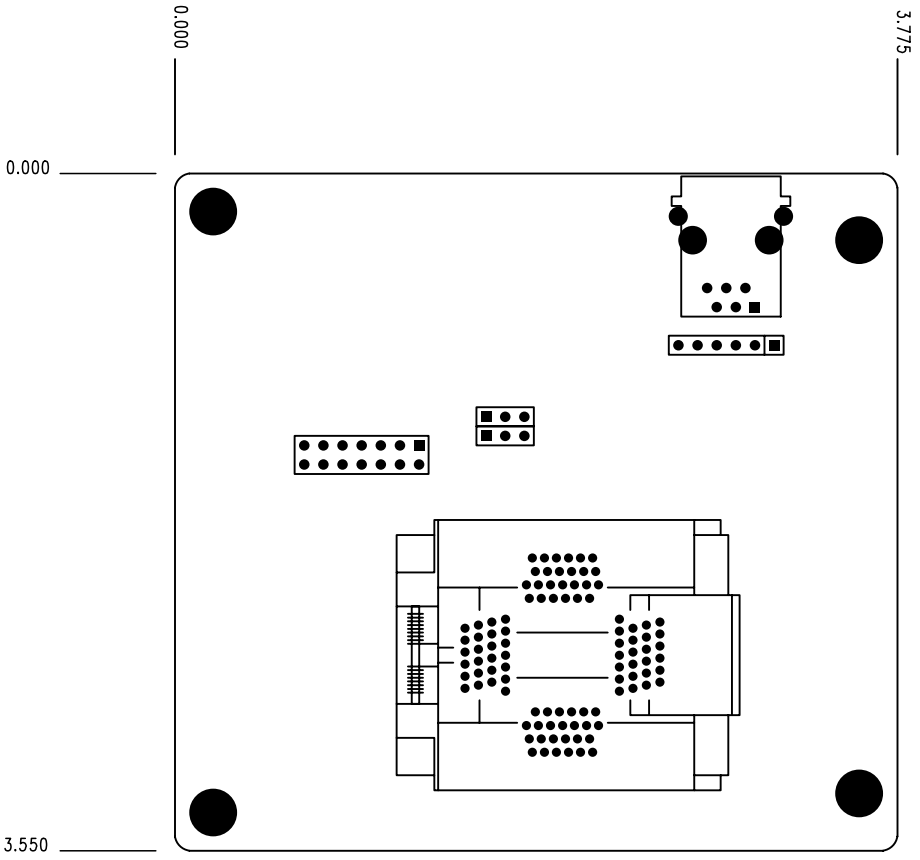
[2] PSPM E Rev A supported the PIC24FJ256GB110. However, the GB210's additional RAM memory was too irresistible, and so PSPM E was revised to support the smaller package Microchip uses on the GB210 part. Thus, Rev B is the first public release of PSPM E.

PHYSICAL CHARACTERISTICS

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Mass				68		g
Height of components above PCB					19	mm
Height of components below PCB[3]					3	mm
PCB width	Same size as CubeSat Kit Module			90		mm
PCB length				96		mm
PCB thickness				1.6		mm

SIMPLIFIED MECHANICAL LAYOUT [4]

PSPM E is implemented on PCB that is the same size as a CubeSat Kit module, as shown below.



[3] Not including connector H1.
[4] Dimensions in inches.

ELECTRICAL CHARACTERISTICS

(T = 25ºC, +5V bus = +5V unless otherwise noted)

Parameter	Conditions / Notes	Symbol	Min	Typ	Max	Units
Reset voltage	**+5V_SYS** reduced until MCU resets	V_{RESET_MAX}			3.1	V
Operating Voltage		V_{CC}		3.3		V
SD Card Voltage		V_{CC_SD}		3.3		V
Operating current	Typical operation[5]	I_{OP}		20		mA
	All control outputs inactive, PSPM asleep	I_{SLEEP}		TBD	TBD	µA
Primary crystal frequency		f_{CLK_OSC}	8.000 ± 0.01			MHz
Secondary crystal frequency		f_{CLK_SOSC}	32.768 ± 0.001			kHz
Overcurrent trip point for **VCC**	Set by **R3**	I_{TRIP_VCC}		220		mA
Time to switch between **+5V_SYS** and **+5V_USB** power sources	Automatic				1	µs

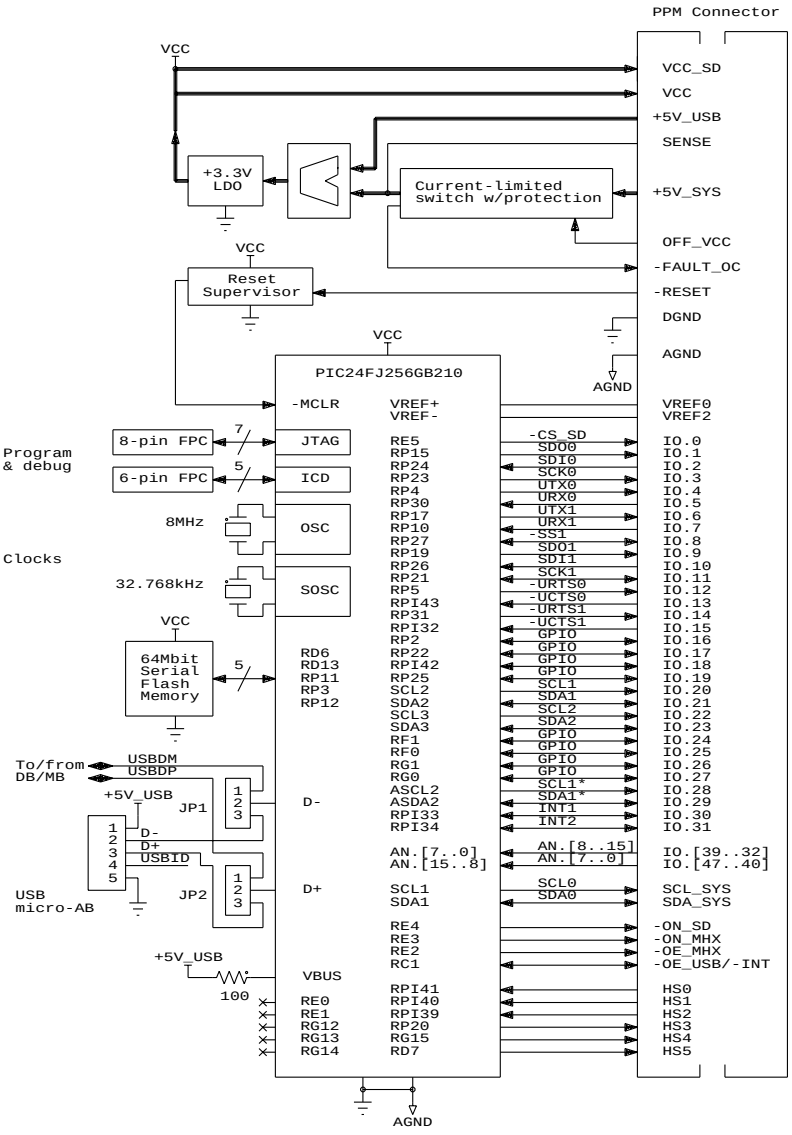
[5] Running CubeSat Kit test\test1 application v1.2.2.

BLOCK DIAGRAM

PSPM E provides regulated and current-limited +3.3V power, internal or external USB connections, an external POR/BOR reset supervisor, JTAG and ICD interfaces for programming and debugging, two clock sources, an external high-speed 64Mbit serial Flash memory, connections to all 48 I/O pins of the PPM connector, dedicated DB control and radio handshaking signals, a single-point analog/digital ground, and a careful assignment of the mappable and non-mappable PIC24 peripherals to the PPM connector and CubeSat Kit bus.

PSPM E accepts a PIC24FJ256GB210 via a 100-pin clamshell ZIF socket, permitting the simple replacement of the processor should inadvertent damage to it occur.

A few of the PIC24's 100 pins are not used.



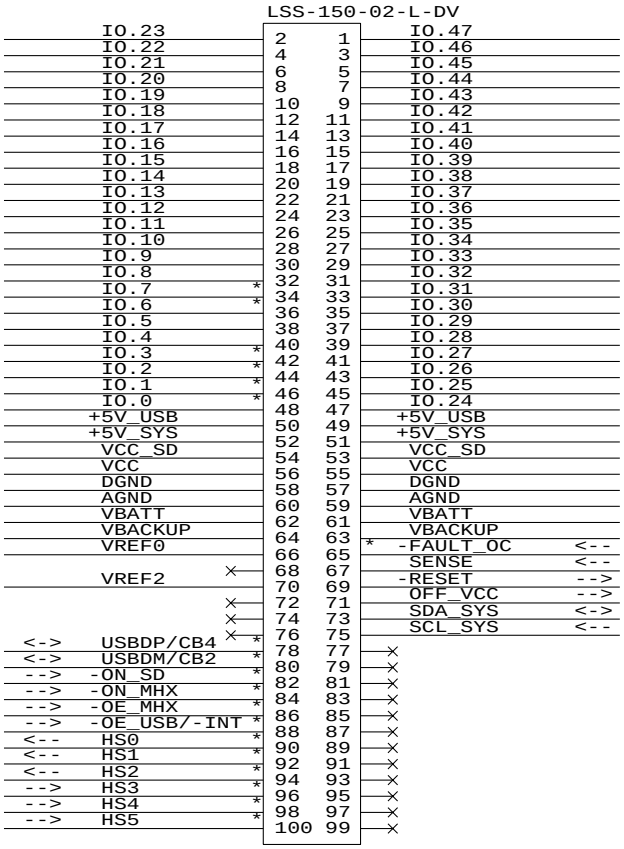
PPM PIN DESCRIPTIONS

The PPM connector **H1** connects the PSPM to resources residing on the DB and to resources accessible via the CubeSat Kit Bus connector.[6]

Those signals that are connected directly to the PPM connector and to the CubeSat Kit Bus connectors are tagged under the CSKB label below.[7] Signals marked with an '*' are associated with dedicated peripherals on the DB. They may also be used with off-board peripherals through the proper use of DB peripheral enables and DB power control.

The *potential* for a pin's function is described by the I/O field. The *recommended usage* (as a digital or analog input or output, or as a power pin) is listed in the Description field. I/O pins can generally be configured as general-purpose I/O if the recommended usage is not desired.

Inputs are signals *from* the DB *to* the PSPM's processor **U1** or other circuitry. *Outputs* are signals *from* the PSPM's processor **U1** or other circuitry *to* the DB.



[6] Not included. DBs are purchased separately from PPMs.

[7] The CubeSat Kit's system peripherals are numbered from 0 onwards (e.g., UART0, SPI0, etc.), and this nomenclature is used when referring to a PPM or CSK bus signal. The PIC24's peripheral nomenclature begins with 1 (e.g., U1, SPI1, etc.), and is used when referring to peripherals, signals and registers internal to the PIC24.

PPM PIN DESCRIPTIONS – I/O

Name	Pin	I/O	CSKB	Description
IO.0	H1.48	I/O	•	**-CS_SD**. Controls SD Card interface. From **RE5** (**U1**.3). *Part of the DB's SD card interface. **RE5** is normally configured as a simple output.*
IO.1	H1.46	I/O	•	**SDO0**. SPI0 (master) data out. From **RP15** (**U1**.53). *Part of the DB's SD card interface. **RP15** is normally configured as output function SDO1.*
IO.2	H1.44	I/O	•	**SDI0**. SPI0 (master) data in. To **RP24** (**U1**.76). *Part of the DB's SD card interface. **RP24** is normally configured as input function SDI1.*
IO.3	H1.42	I/O	•	**SCK0**. SPI0 clock. From **RP23** (**U1**.77). *Part of the DB's SD card interface. **RP23** is normally configured as output function SCK1OUT.*
IO.4	H1.40	I/O	•	**UTX0**. Tx0 data out. From **RP4** (**U1**.69). ***RP4** is normally configured as output function U1TX.*
IO.5	H1.38	I/O	•	**URX0**. Rx0 data in. To **RP30** (**U1**.52). ***RP30** is normally configured as input function U1RX.*
IO.6	H1.36	I/O	•	**UTX1**. Tx1 data out. From **RP17** (**U1**.50). *Part of the DB's MHX/USB interface. **RP17** is normally configured as output function U2TX.*
IO.7	H1.34	I/O	•	**URX1**. Rx1 data in. To **RP10** (**U1**.49). *Part of the DB's MHX/USB interface. **RP10** is normally configured as input function U2RX.*
IO.8	H1.32	I/O	•	**-SS1**. SPI1 slave select. From **RP27** (**U1**.14). *Part of the second SPI interface. **RP27** is normally configured as output function SS2OUT/-SS2. Can also be used as general-purpose I/O.*
IO.9	H1.30	I/O	•	**SDO1**. SPI1 (master) data out. From **RP19** (**U1**.12). *Part of the second SPI interface. **RP19** is normally configured as output function SDO2. Can also be used as general-purpose I/O.*
IO.10	H1.28	I/O	•	**SDI1**. SPI1 (master) data in. To **RP26** (**U1**.11). *Part of the second SPI interface. **RP26** is normally configured as input function SDI2. Can also be used as general-purpose I/O.*
IO.11	H1.26	I/O	•	**SCK1**. SPI1 clock. From **RP21** (**U1**.10). *Part of the second SPI interface. **RP21** is normally configured as output function SCK2OUT/SCK2. Can also be used as general-purpose I/O.*
IO.12	H1.24	I/O	•	**-URTS0**. UART0 request-to-send. From **RP5** (**U1**.48). *Part of the first UART interface. **RP5** is normally configured as output function -U1RTS. Can also be used as general-purpose I/O.*
IO.13	H1.22	I/O	•	**-UCTS0**. UART0 clear-to-send. To **RPI43** (**U1**.47). *Part of the first UART interface. **RPI43** is normally configured as input function –U1CTS. Can also be used as general-purpose I/O.*
IO.14	H1.20	I/O	•	**-URTS1**. UART1 request-to-send. From **RP31** (**U1**.39). *Part of the second UART interface. **RP31** is normally configured as output function –U2RTS. Can also be used as general-purpose I/O.*
IO.15	H1.18	I/O	•	**-UCTS1**. UART1 clear-to-send. To **RPI32** (**U1**.40). *Part of the second UART interface. **RPI32** is normally configured as input function –U2CTS. Can also be used as general-purpose I/O.*
IO.16	H1.16	I/O	•	General-purpose I/O. To/from **RP2** (**U1**.68).
IO.17	H1.14	I/O	•	General-purpose I/O. To/from **RP22** (**U1**.78).
IO.18	H1.12	I/O	•	General-purpose I/O. To/from **RPI42** (**U1**.79).
IO.19	H1.10	I/O	•	General-purpose I/O. To/from **RP25** (**U1**.81).

IO.20	H1.8	I/O	•	**SCL1**. I2C1 clock. From **SCL2** (**U1**.58). *Part of the second I2C interface.* **SCL2** *is normally configured as an I2C clock output. Can also be used as general-purpose I/O.*
IO.21	H1.6	I/O	•	**SDA1**. I2C1 data. To/from **SDA2** (**U1**.59). *Part of the second I2C interface.* **SDA2** *is normally configured as an I2C data input/output. Can also be used as general-purpose I/O.*
IO.22	H1.4	I/O	•	**SCL2**. I2C2 clock. To/from **SCL3** (**U1**.4). *Part of the third I2C interface.* **SCL3** *is normally configured as an I2C clock output. Can also be used as general-purpose I/O.*
IO.23	H1.2	I/O	•	**SDA2**. I2C2 data. To/from **SDA3** (**U1**.5). *Part of the third I2C interface.* **SDA3** *is normally configured as an I2C data input/output. Can also be used as general-purpose I/O.*
IO.24	H1.47	I/O	•	General-purpose I/O. To/from **RF1** (**U1**.88).
IO.25	H1.45	I/O	•	General-purpose I/O. To/from **RF0** (**U1**.87).
IO.26	H1.43	I/O	•	General-purpose I/O. To/from **RG1** (**U1**.89).
IO.27	H1.41	I/O	•	General-purpose I/O. To/from **RG0** (**U1**.90).
IO.28	H1.39	I/O	•	**SCL1*** I2C1 clock (alternate). To/from **ASCL2** (**U1**.66). *Provides an alternate location for the second I2C interface. If used,* **ASCL2** *is normally configured as an I2C clock output. Can also be used as general-purpose I/O.*
IO.29	H1.37	I/O	•	**SDA1***. I2C1 data (alternate). To/from **ASDA2** (**U1**.67). *Provides an alternate location for the second I2C interface. If used,* **ASCL3** *is normally configured as an I2C data input/output. Can also be used as general-purpose I/O.*
IO.30	H1.35	I/O	•	**INT1**. External interrupt. To **RPI33** (**U1**.18). ***RPI33*** *is normally configured as input function INT1. Can also be used as general-purpose I/O.*
IO.31	H1.33	I/O	•	**INT2**. External interrupt. To **RPI34** (**U1**.19). ***RPI34*** *is normally configured as input function INT2. Can also be used as general-purpose I/O.*
IO.32	H1.31	I/O	•	**AN8**. Analog input 8. To **AN5** (**U1**.20). *Can also be used as general-purpose I/O.*
IO.33	H1.29	I/O	•	**AN9**. Analog input 9. To **AN4** (**U1**.21). *Can also be used as general-purpose I/O.*
IO.34	H1.27	I/O	•	**AN10**. Analog input 10. To **AN3** (**U1**.22). *Can also be used as general-purpose I/O.*
IO.35	H1.25	I/O	•	**AN11**. Analog input 11. To **AN2** (**U1**.23). *Can also be used as general-purpose I/O.*
IO.36	H1.23	I/O	•	**AN12**. Analog input 12. To **AN1** (**U1**.24). Also used for **PGEC** (ICD clock). *Can also be used as general-purpose I/O.*
IO.37	H1.21	I/O	•	**AN13**. Analog input 13. To **AN0** (**U1**.25). Also used for **PGED** (ICD data). *Can also be used as general-purpose I/O.*
IO.38	H1.19	I/O	•	**AN14**. Analog input 14. To **AN6** (**U1**.26). *Can also be used as general-purpose I/O.*
IO.39	H1.17	I/O	•	**AN15**. Analog input 15. To **AN7** (**U1**.27). *Can also be used as general-purpose I/O.*
IO.40	H1.15	I/O	•	**AN0**. Analog input 0. To **AN8** (**U1**.32). *Can also be used as general-purpose I/O.*
IO.41	H1.13	I/O	•	**AN1**. Analog input 1. To **AN9** (**U1**.33). *Can also be used as general-purpose I/O.*
IO.42	H1.11	I/O	•	**AN2**. Analog input 2. To **AN10** (**U1**.34). *Can also be used as general-purpose I/O.*
IO.43	H1.9	I/O	•	**AN3**. Analog input 3. To **AN11** (**U1**.35). *Can also be used as general-purpose I/O.*
IO.44	H1.7	I/O	•	**AN4**. Analog input 4. To **AN12** (**U1**.41). *Can also be used as general-purpose I/O.*

IO.45	H1.5	I/O	•	**AN5**. Analog input 5. To **AN13** (**U1**.42). *Can also be used as general-purpose I/O.*
IO.46	H1.3	I/O	•	**AN6**. Analog input 6. To **AN14** (**U1**.43). *Can also be used as general-purpose I/O.*
IO.47	H1.1	I/O	•	**AN7**. Analog input 7. To **AN15** (**U1**.44). *Can also be used as general-purpose I/O.*

PPM PIN DESCRIPTIONS – Power

Name	Pin	I/O	CSKB	Description
+5V_USB	H1.49 H1.50	–	•	+5V USB power. From USB host. Powers PSPM.
+5V_SYS	H1.51 H1.52	–	•	+5V system power. From EPS or external +5V connector. Powers PSPM.
VCC_SD	H1.53 H1.54	–		+3.3V SD Card power. From PSPM's **VCC**.
VCC	H1.55 H1.56	–		+3.3V PSPM power, DB power and I/O level. From PSPM LDO **U4** using **+5V_SYS** and/or **+5V_USB**.
DGND	H1.57 H1.58	–	•	Digital ground.
AGND	H1.59 H1.60	–	•	Analog ground.
VBATT	H1.61 H1.62	–	•	Not connected.
VBACKUP	H1.63 H1.64	–	•	Not connected.

PPM PIN DESCRIPTIONS – Analog References

Name	Pin	I/O	CSKB	Description
VREF0	H1.66	–	•	Positive analog voltage reference. To/from **VREF+** (**U1**.29).
VREF1	H1.68	–	•	Not connected.
VREF2	H1.70	–	•	Negative analog voltage reference. To/from **VREF–** (**U1**.28).

PPM PIN DESCRIPTIONS – Reserved

Name	Pin	I/O	CSKB	Description
RSVD0	H1.72	–	•	Not connected. Reserved for future use.
RSVD1	H1.74	–	•	Not connected. Reserved for future use.
RSVD2	H1.76	–	•	Not connected. Reserved for future use.

PPM PIN DESCRIPTIONS – DB-Specific

Name	Pin	I/O	CSKB	Description
CB4	H1.78	I/O		Not appropriate for use with PSPM E.
USBDP				USB **D+** signal. Active when a jumper is placed across **JP2.**1 & **JP2.**2. Connects **U1.**57 directly to USB connector on the DB. Requires that the USB-to-serial converter on the DB be disabled and configured appropriately to avoid conflicts.
CB2	H1.80	I/O		Not appropriate for use with PSPM E.
USBDM				USB **D–** signal. Active when a jumper is placed across **JP1.**1 & **JP1.**2. Connects **U1.**56 directly to USB connector on the DB. Requires that the USB-to-serial converter on the DB be disabled and configured appropriately to avoid conflicts.
–ON_SD	H1.82	O		Control signal for SD Card power. From **RE4** (**U1**.100). Active LOW, pulled high on the DB. When active, enables **VCC_CARD** on the DB, thereby powering SC Card socket and

				SD Card level translators / isolators. *Normally configured as a digital output.*
-ON_MHX	H1.84	O		Control signal for MHX socket power. From **RE3** (**U1**.99). Active LOW, pulled high on the DB. When active, enables **PWR_MHX** on the DB, thereby powering MHX socket and MHX level translators / isolators. *Normally configured as a digital output.*
-OE_MHX	H1.86	O		Control signal for MHX interface. From **RE2** (**U1**.98). Active LOW, pulled high on the DB. When active, enables signals to pass through MHX level translators / isolators. *Normally configured as a digital output.*
-OE_USB	H1.88	O		Control signal for USB interface. From **RC1** (**U1**.6). Active LOW, pulled high on the DB. When active, enables signals to pass through USB level translators / isolators. *Normally configured as a digital output.*
-INT		I		Output from RTC's -IRQ open-collector output. To **RPI38** (**U1**.6). When properly configured, can be used to interrupt Processor via DB RTC. *Normally configured as a digital input with change-on input interrupt capability.*
HS0	H1.90	I		Handshake signal. -RTS (USB) or -CTS (MHX). To **RPI41** (**U1**.9). *Can be configured as an external interrupt to **U1** or input handshake signal via its Peripheral Pin Select. Requires that **R10** be fitted on the DB.*
HS1	H1.92	I		Handshake signal. -DTR (USB) or -DSR (MHX). To **RPI40** (**U1**.8). *Can be configured as an external interrupt to **U1** or input handshake signal via its Peripheral Pin Select. Requires that **R11** be fitted on the DB.*
HS2	H1.94	I		Handshake signal. -PWE (USB) or -DCD (MHX). To **RPI39** (**U1**.7). *Can be configured as an external interrupt to **U1** or input handshake signal via its Peripheral Pin Select. Requires that **R12** be fitted on the DB.*
HS3	H1.96	O		Handshake signal. -CTS (USB) or -RTS (MHX). From **RP20** (**U1**.82). *Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that **R75** be fitted on the DB.*
HS4	H1.98	O		Handshake signal. -RI (USB) or -DTR (MHX). From **RG15** (**U1**.1). *Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that **R76** be fitted on the DB.*
HS5	H1.100	O		Handshake (reset) signal. -RST (USB) or -RST (MHX). From **RD7** (**U1**.84). *Can be configured as an output handshake signal via its Peripheral Pin Select. Requires that **R77** be fitted on the DB.*

PPM PIN DESCRIPTIONS – Control & Status

Name	Pin	I/O	CSKB	Description
-FAULT_OC	H1.65	O		Open-collector output from PSPM's latchup prevention overcurrent switch. Active LOW. Wire-ORed to **-FAULT_OC** on the DB.
SENSE	H1.67	–	•	Can be used to measure PSPM's current consumption. The current used by the PSPM from a single source is (source – **SENSE**) / 75mΩ. Depends on PSPM implementation.
-RESET	H1.69	I	•	Reset signal to PSPM's reset supervisor. Active LOW.
OFF_VCC	H1.71	I	•	Control signal to PSPM's power circuit(s). Active HIGH.

PPM PIN DESCRIPTIONS – I2C Bus

Name	Pin	I/O	CSKB	Description
SDA_SYS	H1.73	I/O	•	I2C data. To/from **SDA1** (**U1**.67). *Part of the first I2C interface.* **SDA1** *is normally configured as an I2C data input/output. Can also be used as general-purpose I/O.*
SCL_SYS	H1.75	O	•	I2C clock. From **SCL1** (**U1**.66). *Part of the first I2C interface.* **SCL1** *is normally configured as an I2C clock output. Can also be used as general-purpose I/O.*

PPM PIN DESCRIPTIONS – User-defined

Name	Pin	I/O	CSKB	Description
USER0	H1.77	I/O	•	Not connected.
USER1	H1.79	I/O	•	Not connected.
USER2	H1.81	I/O	•	Not connected.
USER3	H1.83	I/O	•	Not connected.
USER4	H1.85	I/O	•	Not connected.
USER5	H1.87	I/O	•	Not connected.
USER6	H1.89	I/O	•	Not connected.
USER7	H1.91	I/O	•	Not connected.
USER8	H1.93	I/O	•	Not connected.
USER9	H1.95	I/O	•	Not connected.
USER10	H1.97	I/O	•	Not connected.
USER11	H1.99	I/O	•	Not connected.

USB INTERFACE

U1 PIC24FJ256GB210 has a built-in USB OTG interface, capable of functioning in either USB Host mode or USB Device mode. Connections can be made through one of two available methods, *local* and *remote*.

For USB Host mode applications, and for general development involving USB Host mode or Device mode, the local USB connector is used. A micro-AB USB receptacle is provided on PSPM E for direct connections from **U1** to USB devices. This feature allows the user to quickly establish a USB connection between **U1** and other USB devices via PSPM E. To utilize the connector, each jumper **JP1** and **JP2** must be connected across its pins 1 and 2. This creates a direct link between **U1**'s D+ and D- pins and the local micro-AB USB receptacle. Additionally, two user-fittable resistors **R9** and **R10** are provided for establishing the logical value for USB OTG's USBID. **R9** sets the USBID high (+5V), and **R10** sets it low (GND). Either one or the other can be used, but not both.[8]

For USB Device mode applications only (e.g., as a USB mass-storage class device, as used in the nanoLab Kit), the USB remote connector is used. The remote connector is the type B USB receptacle on the DB[9], and the USB signals pass to/from PSPM E through the PPM connector down to the DB. In this case, the USB-to-serial converter on the DB must first be disabled to avoid damage to **U1** and/or the DB.[10] To utilize the DB's USB connector, each jumper **JP1** and **JP2** must be connected across its pins 2 and 3. This creates a direct link between **U1**'s D+ and D- pins and the remote type B USB receptacle on the DB.

A graphic is provided on the PSPM E silkscreen to aid in setting the **JP1** and **JP2** jumpers for local or remote USB connections.

U1's **VBUS** signal (**U1**.54) is connected to **+5V_USB** via a 100Ω resistor.

[8] In certain USB OTG modes it may be unnecessary to physically set USBID.

[9] The USB connector on the DB is a type B connector, used exclusively for USB devices and USB OTG Device mode operation.

[10] This is accomplished by holding the FT232R-based USB-to-serial converter in reset, thereby disabling its outputs and preventing it from interfering with USB serial bitstream signals D+ and D-.

SERIAL FLASH MEMORY INTERFACE

PSPM E has an external 64Mbit serial flash memory (SFM) peripheral implemented via an SPI interface to an Atmel AT25DF641 (**U5**). The preferred method of interfacing to **U5** is by using **U1**'s third SPI interface (SPI3) — this will permit a very high-speed interface to **U5**. The pin assignments associated with this interface are listed below.

If the user desires to map SPI3 to the PPM connector instead, the SFM interface pins can be configured as simple I/O, using a software SPI driver to read and write from/to the SFM.

PIN DESCRIPTIONS – Serial Flash Memory Interface

Name	Pin	I/O	Description
-WP	U5.3	I/O	**-WP_SFM**. SFM write-protect function. From **RD6** (**U1**.83). *Part of the third SPI interface. **RD6** is normally configured as a simple output.*
-CS	U5.1	I/O	**-CS_SFM**. SFM chip select. From **RD13** (**U1**.80). *Part of the third SPI interface. **RD13** is normally configured as a simple output.*
SDI	U5.5	I/O	**SDO_SFM**. SPI2 (master) data out. From **RP11** (**U1**.72). *Part of the third SPI interface. **RP11** is normally configured as output function SDO3.*
SDO	U5.2	I/O	**SDI_SFM**. SPI2 (master) data in. From **RP3** (**U1**.70). *Part of the third SPI interface. **RP3** is normally configured as input function SDI3.*
SCK	U5.6	I/O	**SCK_SFM**. SPI2 clock. From **RP12** (**U1**.71). *Part of the third SPI interface. **RP12** is normally configured as output function SCK3OUT.*

CONNECTORS

Item	Description	Source	Part Number	Application
1	100-pin, hermaphroditic	Samtec	LSS-150-02-L-DV	PPM connector (PSPM-specific, +6mm)

This connector information is provided for reference only.

PROGRAMMING & DEBUGGING

PSPM E provides two interfaces for programming and debugging – the popular and low-cost In-Circuit Debugging (ICD) interface, and a JTAG interface. The ICD interface is implemented via a 6-pin RJ11 modular connector on the PSPM. The JTAG interface is implemented via a 0.100" pitch header on the PSPM.

6-pin RJ11[11] 6P6C modular connector **J1** is for the ICD. Customers can connect either a traditional Microchip® ICD like the ICD2 or ICD3, with its 6-pin modular cable, or a Microchip PICKit®, to the PSPM's 6-pin 1x6 0.100" pitch inline header **J3**. **PGEC** (**U1**.24) and **PGED** (**U1**.25) are used as the clock/data pair for the ICD. No isolation from these signals to the CSK bus is provided – therefore care should be taken in connecting circuitry to **IO.36** and **IO.37** of the CSK bus.

14-pin 2x7 0.100" pitch dual-inline header **J2** is for JTAG, and is compatible with 14-conductor IDC ribbon cables for use with Microchip's Real ICE™ and other compatible ICEs.

NOTES

The PIC24's Peripheral Pin Select system enables the user to place digital peripherals at the selected I/O pins of choice. When PSPM E is fitted with a PIC24FJ256GB210 processor, the peripheral functions (e.g., second and third I2C interfaces, second and third SPI interfaces, third and fourth UART interfaces) beyond those that interact with peripheral hardware on the DB have been arranged in a logical manner on the PPM connector, and will correspond to the same arrangement on other PPMs where such additional peripherals present in the processor utilized on that PPM.

[11] Also called RJ25.

Additionally, some mappable PIC24 peripherals (e.g., the third and fourth UARTs) are not assigned pins on the PPM connector. The user can bring them to the CubeSat Kit bus – and thereby to any CubeSat Kit-compatible modules – by mapping them to unused **RP**/**RPI** pins (e.g., those on **IO.16** through **IO.19**), or to other **RP**/**RPI** pins of choice. In all cases, **IO.0** through **IO.7** should remain with the peripheral assignments outlined above, as they correspond to resources on the CSK DB.

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744 Naples Street
San Francisco, CA 94112 USA
tel: (415) 584-6360
fax: (415) 585-7948

web: http://www.pumpkininc.com/
email: info@pumpkininc.com

web: http://www.cubesatkit.com/
email: info@cubesatkit.com